



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,825	07/01/2003	Fabrizio Simone Rovati	851763.434	3917
500	7590	09/19/2008		
SEED INTELLECTUAL PROPERTY LAW GROUP PLLC			EXAMINER	
701 FIFTH AVE			WOOD, WILLIAM H	
SUITE 5400			ART UNIT	PAPER NUMBER
SEATTLE, WA 98104			2193	
		MAIL DATE	DELIVERY MODE	
		09/19/2008	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/612,825	<b>Applicant(s)</b> ROVATI ET AL.
	<b>Examiner</b> William H. Wood	<b>Art Unit</b> 2193

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 21 May 2008.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1,2,4-18 and 20-22 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1,2,4-18 and 20-22 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/95/08)  
Paper No(s)/Mail Date \_\_\_\_\_

4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_

5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_

#### **DETAILED ACTION**

Claims 1-2, 4-18 and 20-22 are pending and have been examined.

##### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 22 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly added claim language is not found in the originally filed disclosure. Appropriate correction is required.

##### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-2 and 4-11 are rejected under 35 U.S.C. 102(e) as being anticipated by **Menezes** (USPN 6,950,926).

***Claim 1***

**Menezes** disclosed a process for executing programs on at least one processor having a given instruction set architecture, characterized in that it comprises the operations of:

compiling the program to be executed and translating said program into native instructions of said instruction set architecture, organizing the instructions deriving from the translation of said program into respective bundles arranged in order of successive bundles, each bundle grouping together instructions adapted to be executed in parallel by said at least one processor (*column 3, lines 24-31; column 5, lines 2-4, “concurrently”*);

separating said bundles of instructions in respective sub-bundles by detecting a value of a binary symbol encoded in one of the instructions deriving from the translation of the program to be executed of the respective bundle (*column 5, line 63 to column 6, line 10, “it is possible that an instruction in the second set has a data dependency on an instruction in the first set. A neutral instruction can be used to describe the*

*interdependency not only among the instructions in a set but also between sets", "single bit or value"; it is translated at least at the time the neutral instruction is added, this instruction provided the sub-grouping), said sub-bundles identifying a first set of instructions, which must be executed before the instructions belonging to the next bundle of said order, and a second set of instructions that can be executed both before and in parallel with respect to the instructions belonging to said next bundle of said order, it being possible for at least said second set of instructions to be the null set (column 4, lines 16-27; column 4, line 60 to column 5, line 6; column 5, line 59 to column 6, line 15; sub-bundle being instructions in first set required to execute before the second set/bundle);*

defining a sequence of execution of the instructions of said sub-bundles in successive operating cycles of said at least one processor, while preventing, in assigning each sub-bundle to an operating cycle of the processor, simultaneous assignment, to the same operating cycle, of two sub-bundles corresponding to instructions belonging to said first set of two successive bundles of said order (column 6, lines 11-15); and

executing said instructions on at least one said processor respecting said execution sequence (column 3, line 22).

Claim 2

**Menezes** disclosed the process according to claim 1, characterized in that it comprises the operation of selectively varying the overall length of instruction executed for each

cycle by said at least one processor (*column 3, line 4, VLIW*).

Claim 4

**Menezes** disclosed the process according to claim 3, characterized in that it comprises the operations of:

detecting when one between said first set and said second set is the null set (*column 4, line 62 to column 5, line 1*); and

inserting in the respective sub-bundle a fictitious instruction which does not imply any execution of operations (*column 3, line 60 to column 4, line 15; figure 1*).

Claim 5

**Menezes** disclosed the process according to claim 1, characterized in that it comprises the operation of identifying the instructions belonging to a sub-bundle of said first set and of said second set by means of two distinct binary symbols which identify the last instruction of the respective sub-bundle (*column 4, lines 13-15, "succeed ... the set"; column 4, lines 28-43, opcode and operand of the neutral instructions*).

Claim 6

**Menezes** disclosed the process according to claim 1, for executing programs on a multiprocessor system comprising a plurality of processors having said instruction-set architecture (*column 1, lines 14-17, multiple execution units*), characterized in that it comprises the operations of:

instantiating the processors of said plurality with respective degrees of parallelism of execution with at least two different values of said parallelism of execution in the context of said plurality (*column 1, lines 49-54; multiple execution units might all be executing in parallel or maybe just some are executing in parallel*); and

selectively distributing execution of the instructions of said sequence of execution among the processors of said plurality, the instructions of said sequence of execution being directly executable by the processors of said plurality in conditions of binary compatibility (*column 1, lines 14-17, multiple execution units; column 1, lines 49-54; distributed to the multiple execution units*).

**Claim 7**

**Menezes** disclosed the process according to claim 6, characterized in that it comprises the operation of selectively distributing the execution of the instructions of said sequence among the processors of said plurality, dynamically distributing the computational load of said processors (*column 1, lines 14-17, multiple execution units to be selected for the instructions*).

**Claim 8**

**Menezes** disclosed the process according to claim 6, characterized in that it comprises the operation of selectively distributing the execution of the instructions of said sequence among said processors of said plurality with the criterion of equalizing the operating frequency of the processors of said plurality (*column 1, lines 14-17, multiple*

*execution units).*

*Claim 9*

**Menezes** disclosed the process according to claim 6, characterized in that it comprises the operation of performing a process of control executed by at least one of the processors of said plurality so as to equalize its own workload with respect to the other processors of said multiprocessor system (*column 1, lines 14-17, multiple execution units; figure 3, elements 201 and 203, equalized with respect to each other*).

*Claim 10*

**Menezes** disclosed the process according to claim 9, characterized in that it comprises the operation of drawing up a table accessible by said control process, said table having items chosen from the group made up of:

    a list of processes that are being executed or are suspended on any processor of said plurality of processors (*column 6, lines 11-15*);

    the progressive number thereof according to the order of activation;

    the percentage of maximum power of the processor that is used by said process;

    the execution time;

    the amount of memory of the system used by said process to be able to execute the function for which it is responsible;

    the processor on which the process currently resides; and

the address of the portion of memory in which the data and the instructions are stored (*column 6, lines 29-45*).

**Claim 11**

**Menezes** disclosed a processor system, preferably of a multiprocessor type, configured for operating with the process according to claim 1 (*column 4, lines 62-65*).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 12-18 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tulai, Alexander (UK Patent Application)** in view of **Menezes (USPN 6,950,926)**.

**Claim 12**

**Tulai** disclosed a process of executing programs on a system having a plurality of processors comprising:

organizing said instruction sets into respective groups, each group having a predetermined priority for execution in a given processor of said plurality (*page 3, lines 20-23; page 6, lines 17-18*);

encoding said instructions for execution on said processors (*page 3, lines 20-23; page 6, lines 17-18*); and

providing in each encoded instruction a designated number of initial bits identifying said predetermined priority of the instruction set (*page 3, lines 20-23; page 6, lines 17-18*).

**Tulai** did not explicitly state compiling the program to be executed and translating.

**Menezes** demonstrated that it was known at the time of invention to compile a program (column 1, lines 59-60; column 3, lines 26-31; and column 4, lines 59-62) and translate a program (column 1, line 58). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the multi-processor parallel execution system of **Tulai** with compiling a program and translating the program into the instruction sets of the plurality of processors of **Tulai** as found in **Menezes'** teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to reduce the hardware calculation burden (**Menezes**: column 1, lines 63-65).

**Menezes** demonstrated that it was known at the time of invention to implement separating said groups of instructions into respective sub-bundles, said sub-bundles identifying a first set of instructions, which must be executed before the instructions belonging to the next group, and a second set of instructions that can be executed both before and in parallel with respect to the instructions belonging to said next group, it being possible for at least said second set of instructions to be the null set (column 4, lines 16-27; column 4, line 60 to column 5, line 6; column 5, line 59 to column 6, line 15;

sub-bundle being instructions in first set required to execute before the second set/bundle). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the multi-processor parallel execution system of **Tulai** with compiling a program and organizing the program into dependency relationships for parallel execution as found in **Menezes**' teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to reduce the hardware calculation burden (**Menezes**: column 1, lines 63-65).

*Claim 13*

**Tulai** and **Menezes** disclosed the process of claim 12, wherein the execution of programs comprises directing of the instruction sets to said processors of said plurality according to the priority bits encoded into the said instruction set (**Tulai**: page 3, *lines 20-23; page 6, lines 17-18*).

*Claim 14*

**Tulai** and **Menezes** disclosed the process of claim 12, wherein said priority is determined based on the amount of memory required by each of the processors of said plurality to execute said instruction set (**Tulai**: page 2, *line 24 to page 3, line 2; page 5, lines 22-23; page 6, line 25 to page 7, line 1; page 10, lines 14-19; thus assigning/prioritizing instructions to a processor is based upon memory considerations of those processors*).

Claim 15

**Tulai** and **Menezes** disclosed the process of claim 12, wherein said priority is determined based on the amount of percentage of maximum power required by each of the processors of said plurality to execute said instruction set (*Tulai: page 2, lines 19-21; page 7, lines 7-9; page 10, line 25 to page 11, line 3; thus assigning/prioritizing instructions to a processor is based upon power considerations of those processors*).

Claims 16-18

The limitations of claims 16-18 correspond to the limitations of claims 12-15 and as such are rejected in the same manner. **Menezes** discloses multiple processors (column 1, lines 14-17, multiple execution units for processing; multiple processors are obviously faster than one).

Claim 20

**Tulai** and **Menezes** disclose the system of claim 16 wherein the first processor is further configured to extract indications of sub-bundling of sets of instructions having respective priority values from the instructions and to determine, based on the extracted indications of sub-bundling, a number of instructions to be executed in each cycle (*Menezes: column 1, lines 14-17, multiple execution units for processing; column 5, line 63 to column 6, line 10, "it is possible that an instruction in the second set has a data dependency on an instruction in the first set. A neutral instruction can be used to describe the interdependency not only among the instructions in a set but also between*

*sets"; the number of indicated and then executed by sub-bundling are those to be executed in each cycle; as motivated above).*

*Claim 21*

**Tulai and Menezes** disclose the process of claim 12, further comprising encoding a value of binary symbol in a translated instruction of the program to be executed, the value indicating a boundary between the first sub-bundle and the second sub-bundle of the respective group of instructions (**Menezes**: *column 5, line 63 to column 6, line 10*, "it is possible that an instruction in the second set has a data dependency on an instruction in the first set. A neutral instruction can be used to describe the interdependency not only among the instructions in a set but also between sets", by the neutral instruction; as motivated above).

*Claim 22*

**Tulai and Menezes** disclose the process of claim 12, further comprising encoding a value of a binary symbol into each translated instruction of the program to be executed, the value indicating the respective sub-bundle of the instruction (**Tulai**: *page 2, lines 16-21*).

***Response to Arguments***

Applicant's arguments filed 21 May 2008 have been fully considered but they are not persuasive. Applicant argues: <sup>1)</sup> newly added claim 1 language, "deriving from the

translation of the program to be executed" is not found in the cited prior art, **Menezes** (Arguments: page 8);<sup>2)</sup> group dependencies disprove the cited prior art organizing the instructions into bundles to be executed in parallel (Arguments: page 9);<sup>3)</sup> the cited prior art's use of a neutral instruction does not provide organizing instructions into bundles to be executed in parallel (Arguments: page 9);<sup>4)</sup> **Menezes** fails to disclose separating into sub-bundles using "a value of a binary symbol encoded in one of the instructions" (Arguments: page 10);<sup>5)</sup> inherency requires support to show organizing into bundles for parallel execution and separating into sub-bundles (Arguments: page 10);<sup>6)</sup> **Tulia** and **Menezes** does not organize instructions into groups and further separate the groups into sub-bundles (Arguments: page 11);<sup>7)</sup> no processor disclosed for directing instruction sets to each of the plurality of processors (Arguments: page 11); and<sup>8)</sup> no disclosure of priority based on the maximum power required (Arguments: page 12).

The first issue is addressed in the above rejections. The timing issue of "before" is not present in the claim.

As to the second and third issues, **Menezes** makes clear groups (sets or bundles) of instructions are organized to be executed in parallel (see cited portions of prior art in the above rejections). Regardless of other groupings options that may exist (that may be related to dependencies), there are groups that may be executed in parallel. The claims do not require a separate "organizing" step any further than that which is already provided by a compiler translating and organizing instructions (as compilers do).

Fourth, **Menezes** states, "it is possible that an instruction in the second set has a data dependency on an instruction in the first set" "a neutral instruction can be used to describe the interdependency not only among the instructions in a set but also between sets", "single bit or value" (column 5, line 63 to column 6, line 10). The neutral instruction clearly demonstrates the grouping and sub-grouping information and is part of the bundle.

As to the fifth issue raised by Applicant's, an inherency argument is not being made. **Menezes** delineates groups of instructions and has thus, under the broadest reasonable interpretation of the claim language, bundled or grouped instructions. Applicant is not taking into account there may be multiple manners or mechanisms by which "bundling" may occur.

The sixth issue is addressed above under issues two through five.

In regard to the seventh issue, **Menezes** discloses multiple processors (column 1, lines 14-17, multiple execution units for processing). Motivation is provided by the fact that multiple processors are obviously faster than one.

As to the eighth issue, **Tulai** discloses assigning/prioritizing instructions to a processor is based upon power considerations of those processors (page 2, lines 19-21; page 7, lines 7-9; page 10, line 25 to page 11, line 3), power considerations would therefore be a percentage of the maximum power.

Having addressed Applicant's raised concerns, the rejections are maintained as indicated.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### ***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (571)272-3736. The examiner can normally be reached 10:00am - 4:00pm Tuesday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis A. Bullock Jr. can be reached on (571)272-3759. The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR systems, see <http://pair-direct.uspto.gov>. For questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

/William H. Wood/  
William H. Wood  
Primary Examiner, Art Unit 2193  
September 20, 2008